Integrated Circuit Technology Challenges

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Technology & Manufacturing Group
Technology Strategy
April 27, 2006

Key Messages

Silicon Nanoelectronics is production reality and follows Moore's law

New materials are needed to extend CMOS

Long term: Novel devices will be needed to enhance CMOS

New materials, metrology, and modeling are required

Increased collaboration between Industry, Universities & Gov't is essential!!!

Agenda

Moore's Law

Extending CMOS

Emerging Research Memory Devices

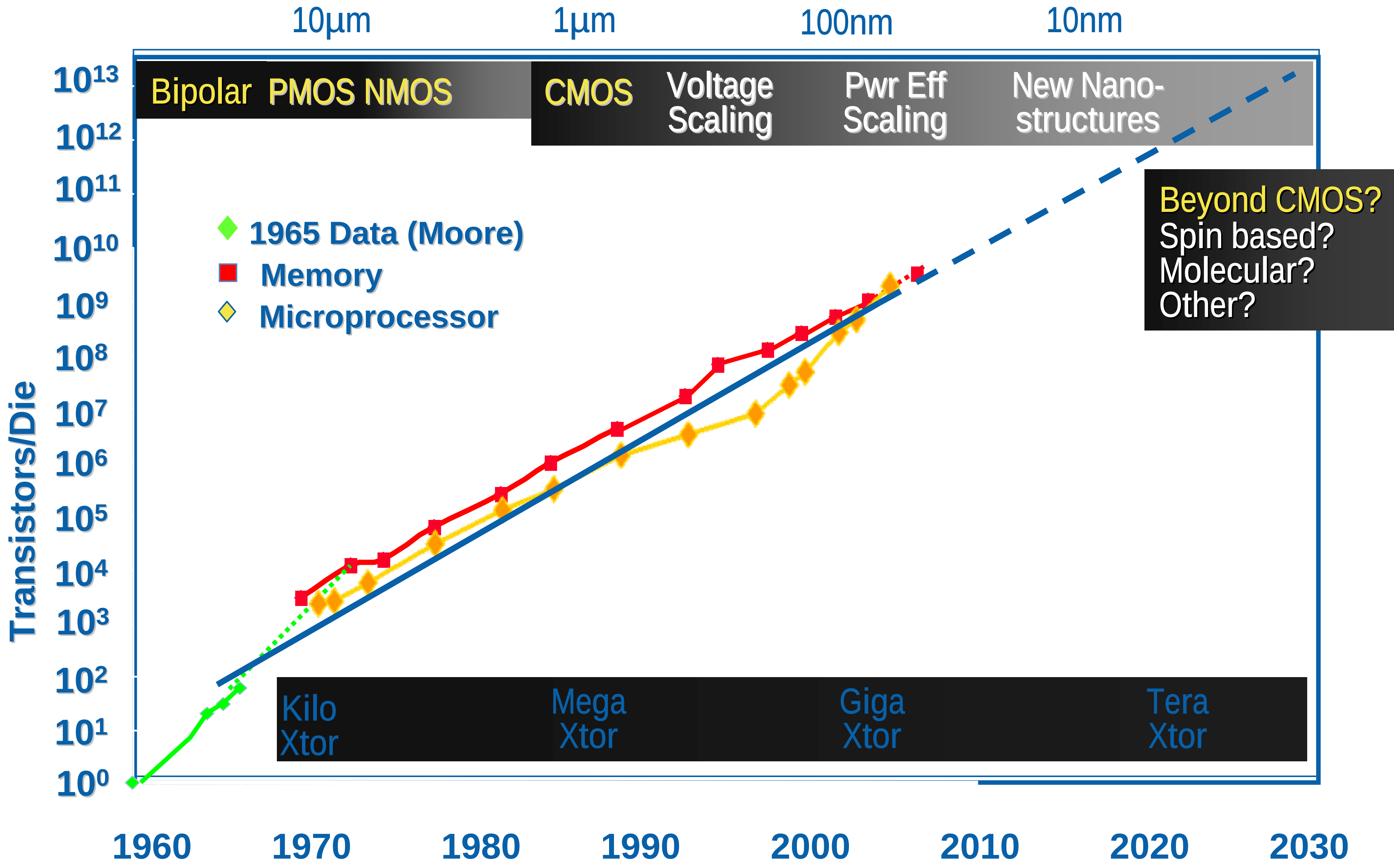
Revolutionary CMOS

Device options to enhance CMOS (Beyond CMOS)

Nanomaterial Challenges

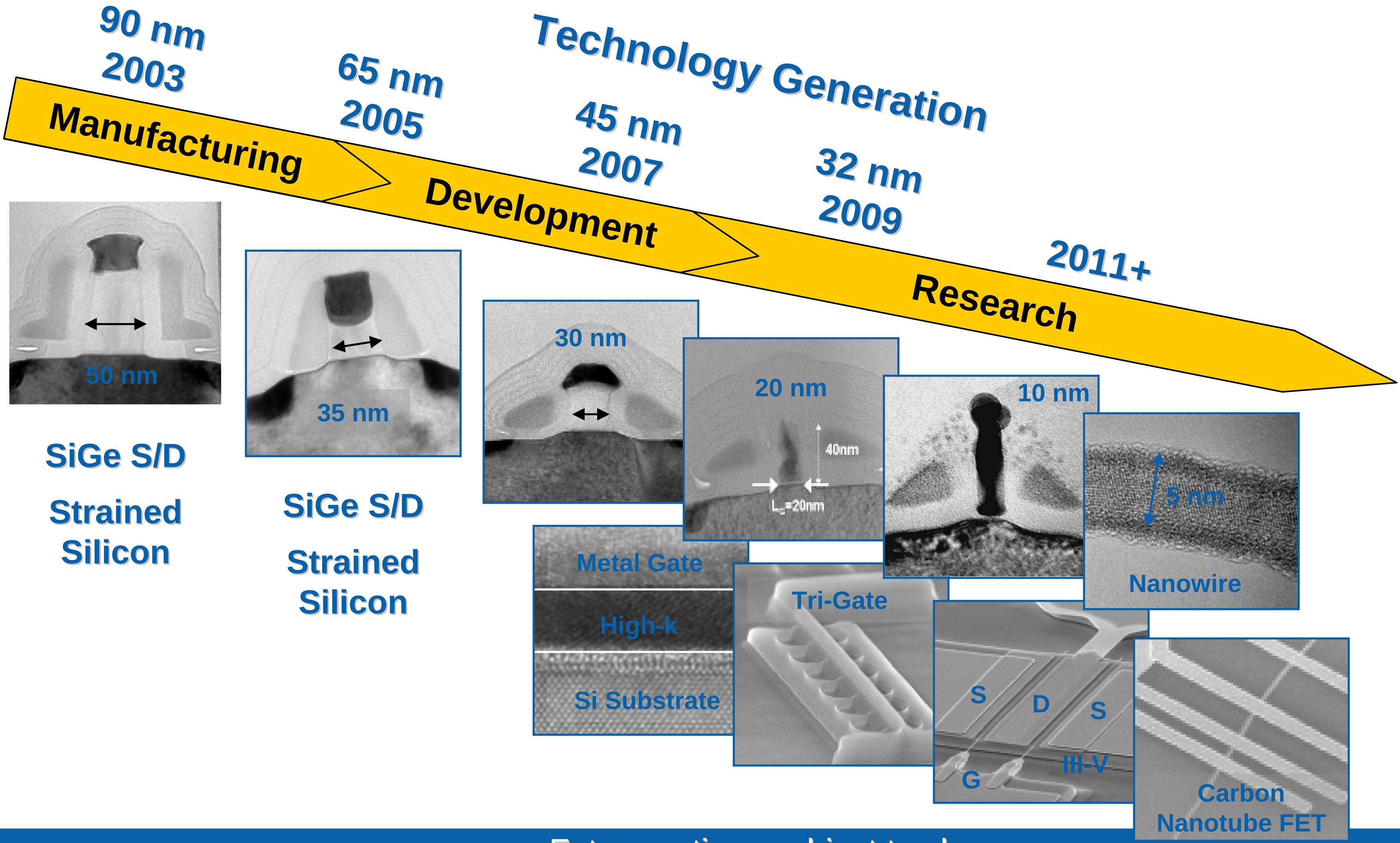
Summary

Moore's Law Will Outlive CMOS



Source: Intel

Innovation-Enabled Pipeline in Place



Technology Generation

90 nm
2003

65 nm
2005

45 nm
2007

32 nm
2009

2011+

Manufacturing

Development

Research

SiGe S/D

Strained Silicon

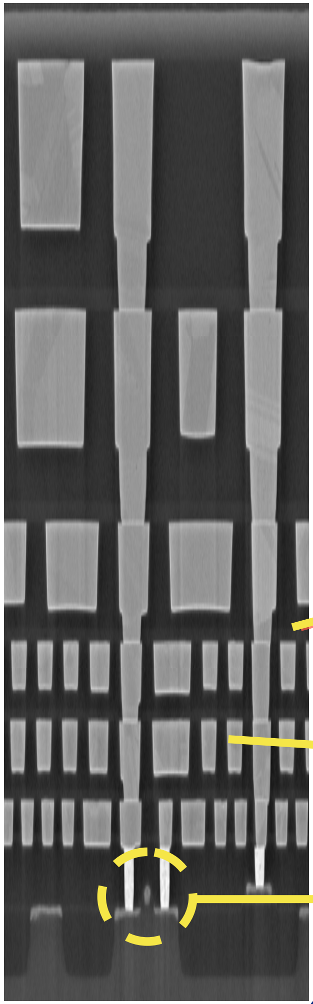
SiGe S/D

Strained Silicon

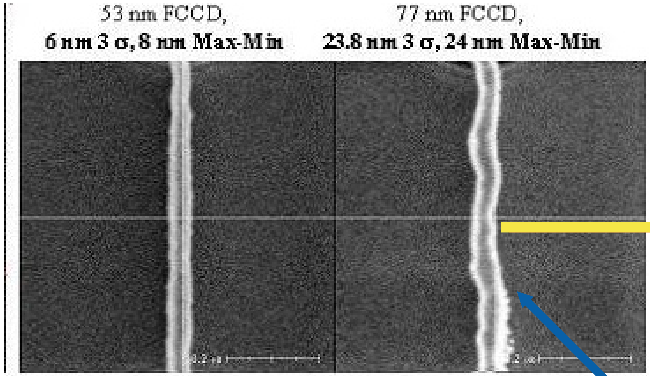
Future options subject to change

Source: Intel

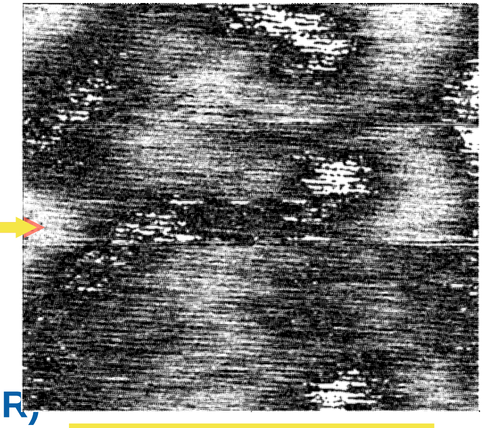
Material Challenges



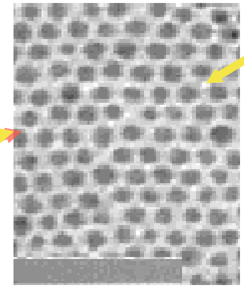
PPT Shrink
Source: Intel



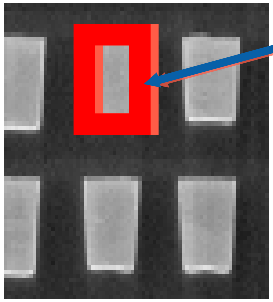
Printed Features: Line Edge Roughness (LER)



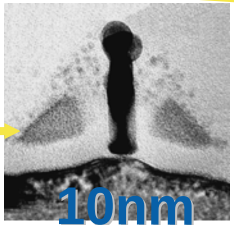
Resist Nano-domains



Low K Interlevel Dielectric
Micelle Assembled….



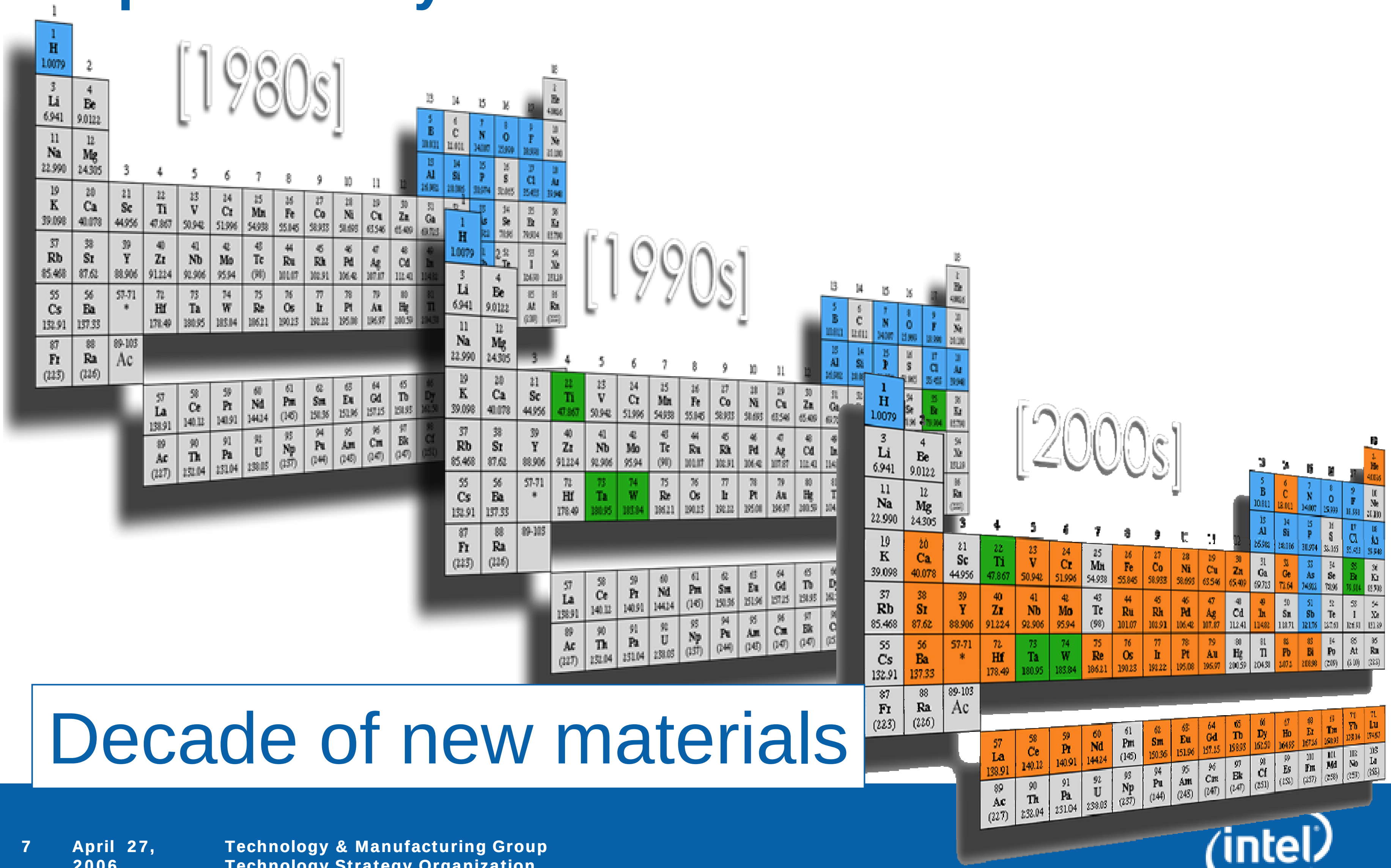
Barrier Layer ~20nm



What Device Next?
What Materials?
How to Assemble?

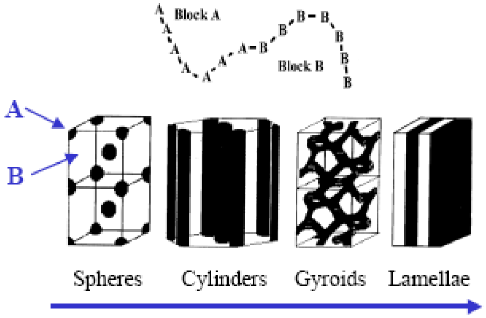
Materials Challenges Everywhere

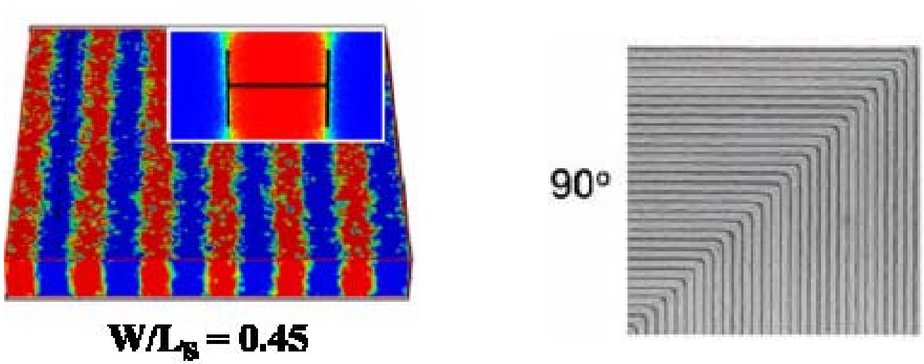
Si Technology: Complexity Increasing Exponentially



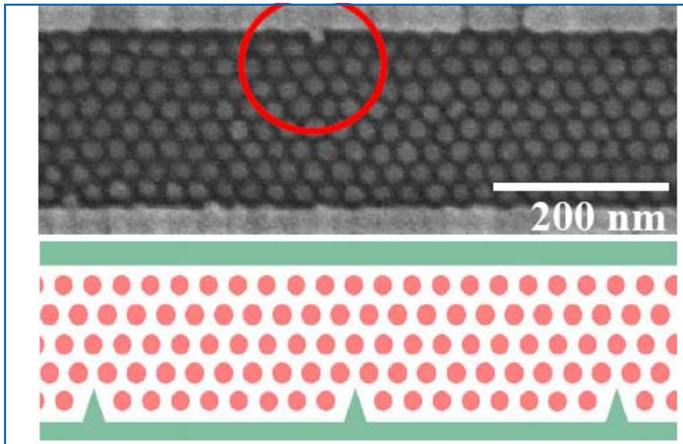
Decade of new materials

Directed Self Assembly Progress





Di-block Copolymer self assembly on patterned Molecular monolayer: Goal reduce LER
P. Nealey, U. Wisc.

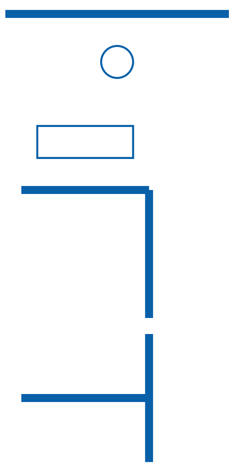


Di-block Copolymer self assembly of magnetic materials in a confined space.
C. Ross, MIT

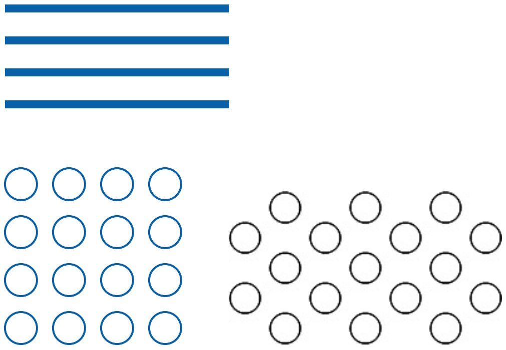
Progress in aligning self assembled structures with lithographically defined structures

Sublithographic Directed Self Assembly Lithography

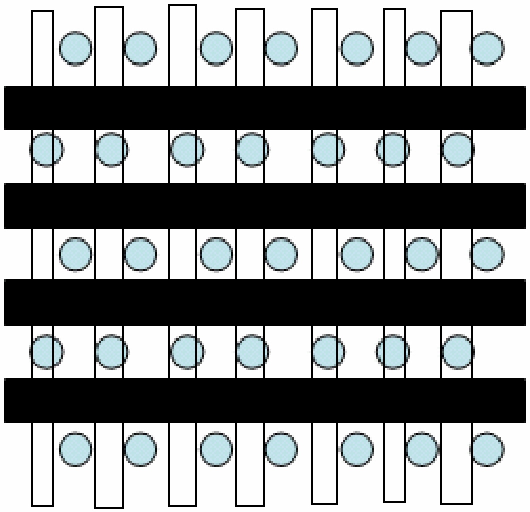
Isolated Sublithographic Features



Periodic features: variable pitch and size on the same layer

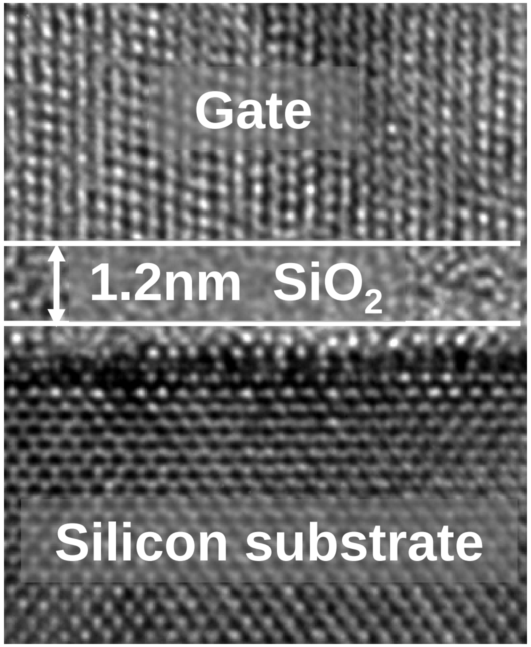


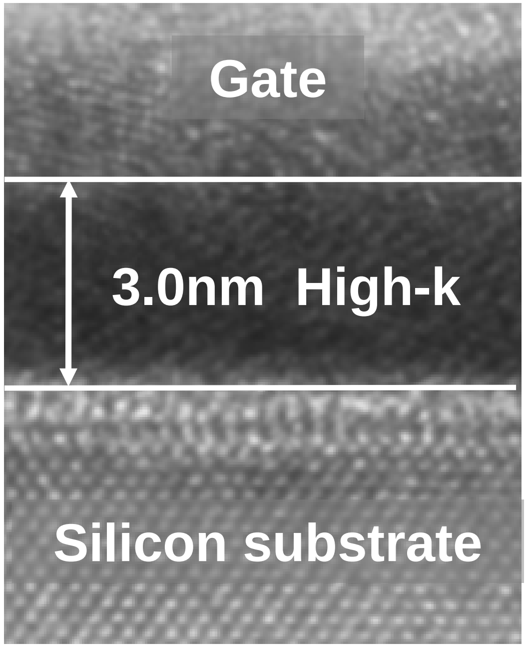
Level to Level Alignment



- Self Assembly may be used in nonaligned applications
- To Extend lithography, the challenges are significant!!

High-k Dielectric reduces leakage substantially



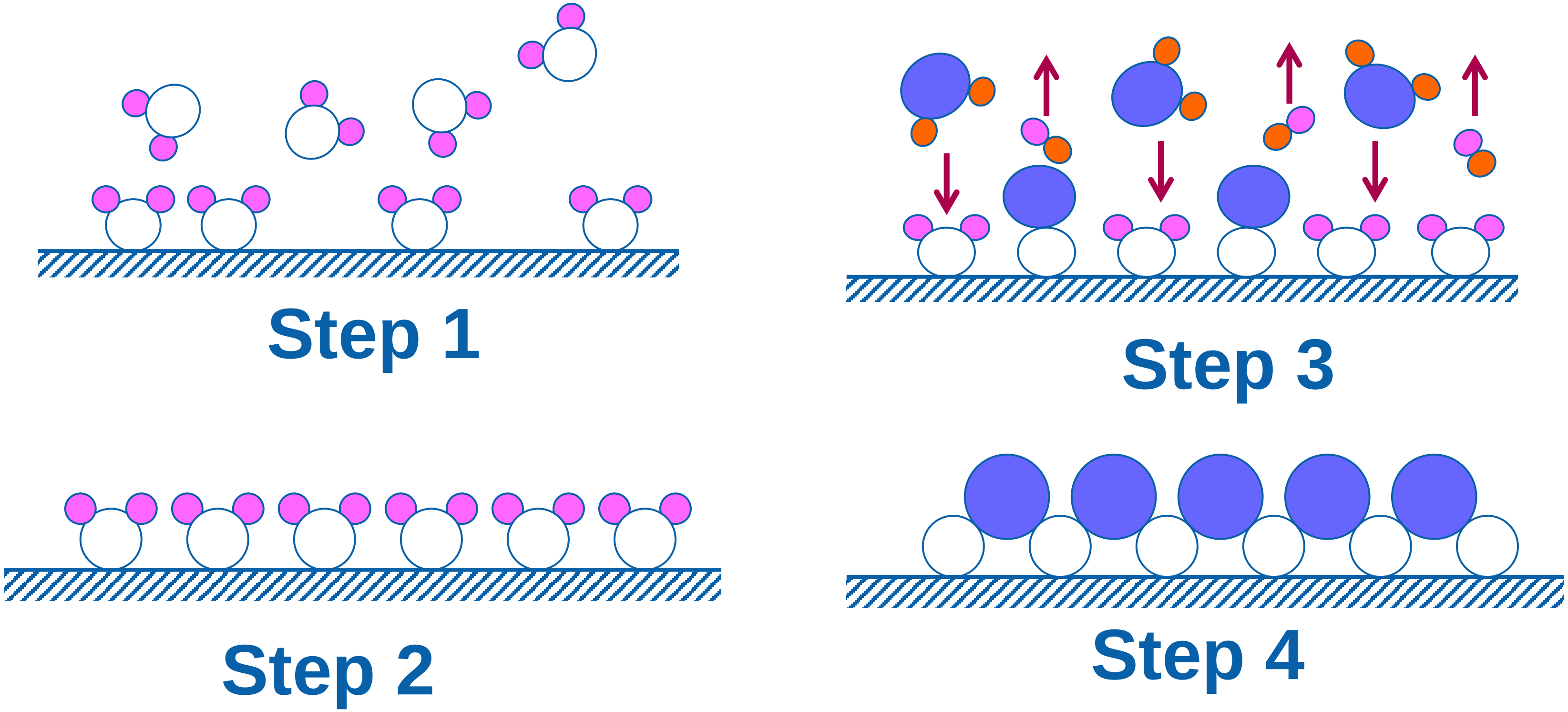


Robert Chau, Nov., 2003

Benefits compared to current process technologies

	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*

High-k Materials Require New Manufacturing Techniques



High-k Materials Are Deposited One Molecular Layer at a Time
Precursors must be Designed for Monolayer Assembly

New Interconnect Materials

Changes Made

Metal lines

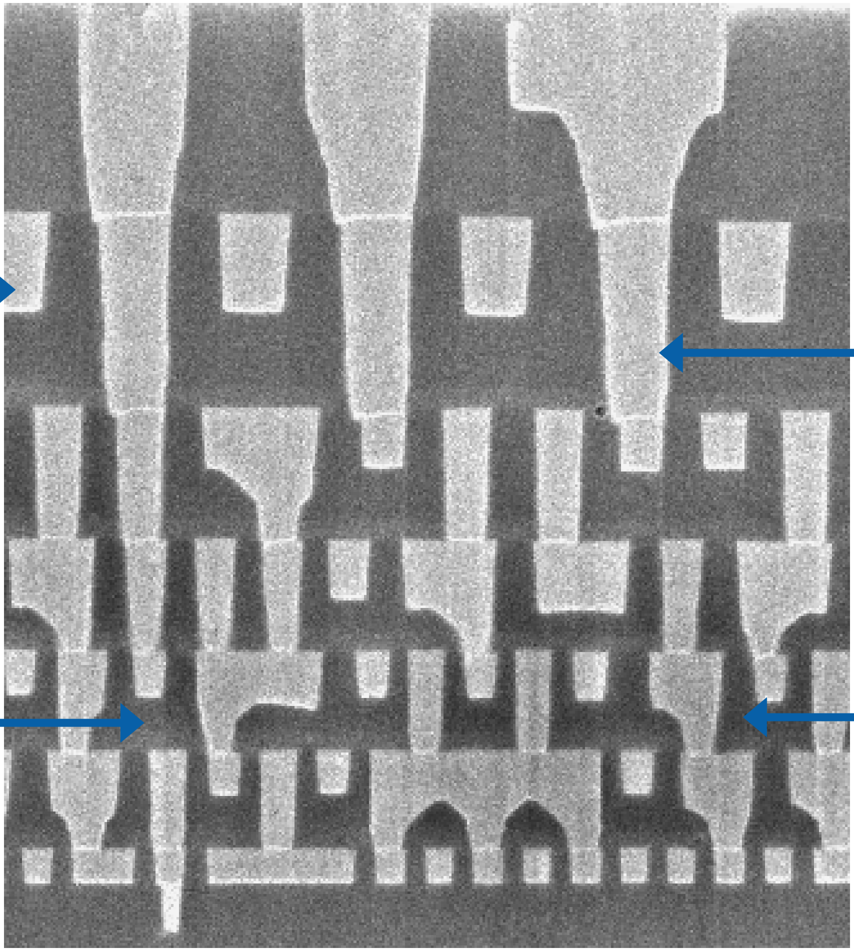
Al → Cu

Insulating dielectric

SiO_2 → SiOF

→ CDO

(low-k)



Interconnects

Future Options

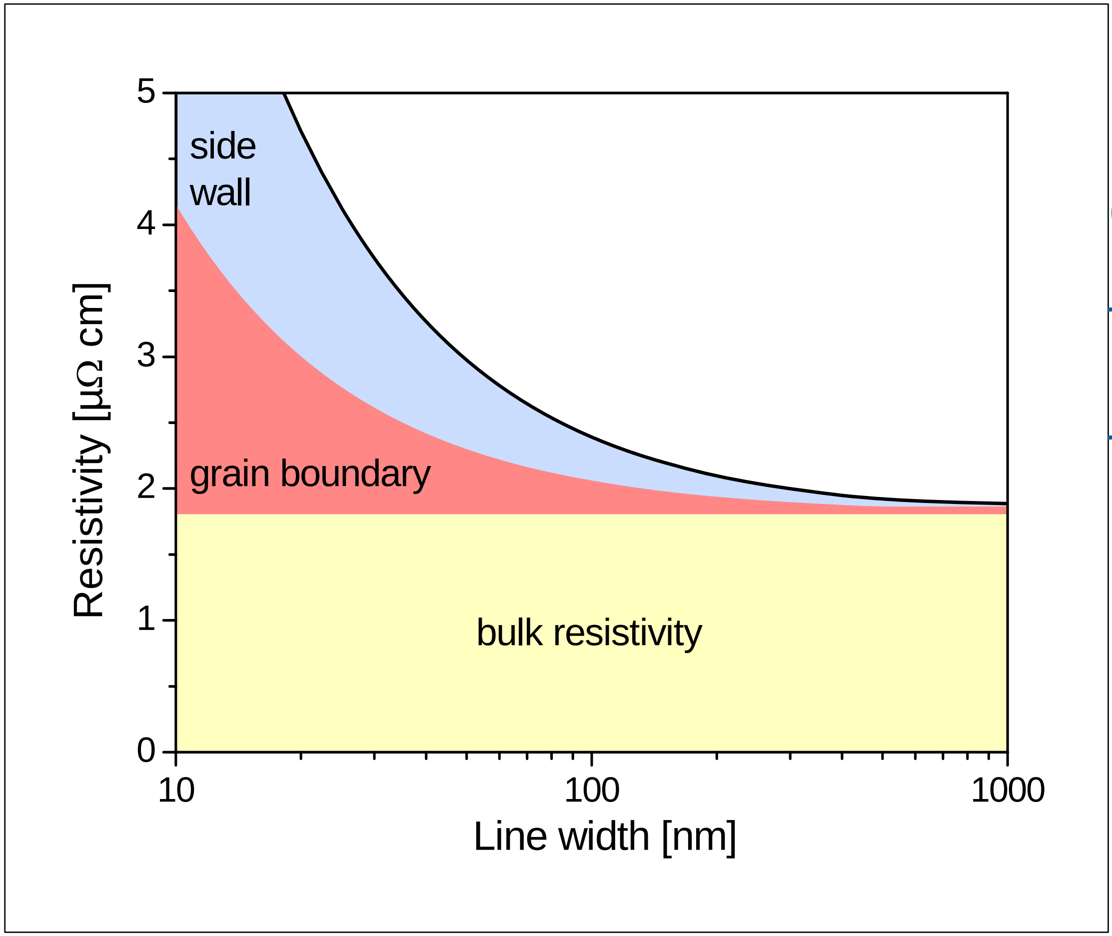
New Thinner Barrier Layers

Ultra Low-k Dielectric

Source: Intel

Lower K Dielectrics Needed

Small Line Conductivity

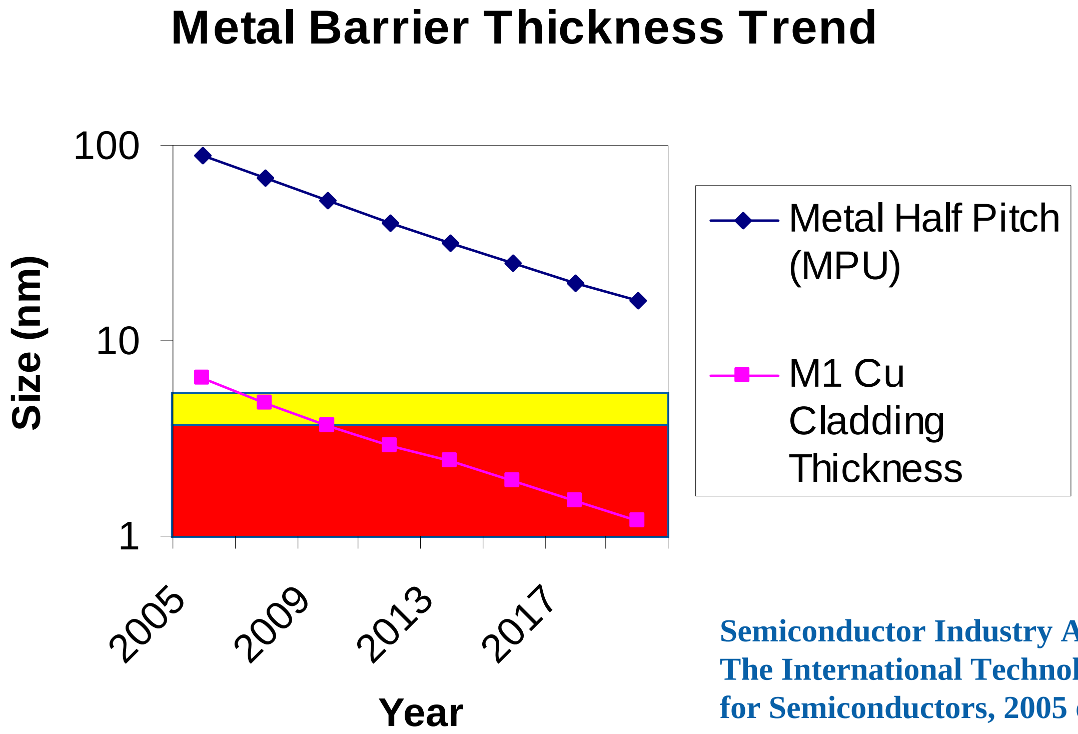


Challenge

- Reduce grain scattering
- Increase grain size
- Reduce sidewall scattering
- Reduce line width roughness
- New smoother materials??

Semiconductor Industry Association
The International Technology Roadmap for Semiconductors, 2005 edition
SEMATECH: Austin, TX, 2005

Cu Barrier Cladding Layer

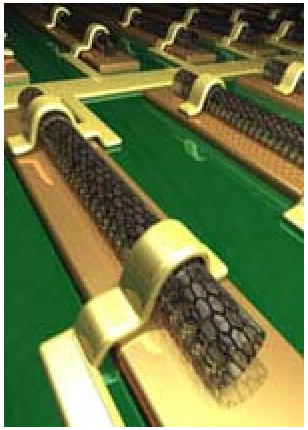


Barrier Options
- •PVD
- •CVD
- •ALD Ti, Ta, W
  Oxides & Nitrides

Novel Materials
Ru, etc

Semiconductor Industry Association
The International Technology Roadmap for Semiconductors, 2005 edition
SEMATECH: Austin, TX, 2005

Could Nanomaterials Extend Interconnect Scaling?



Technology Research News
Oct. 10, 2001

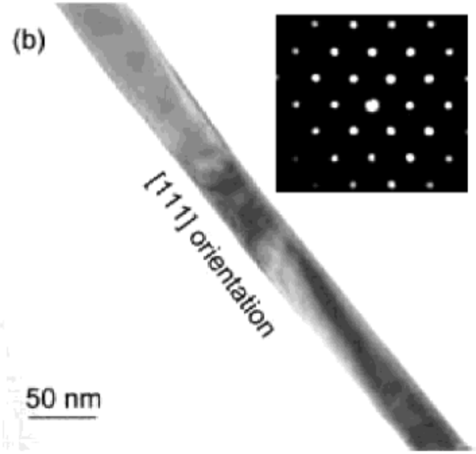
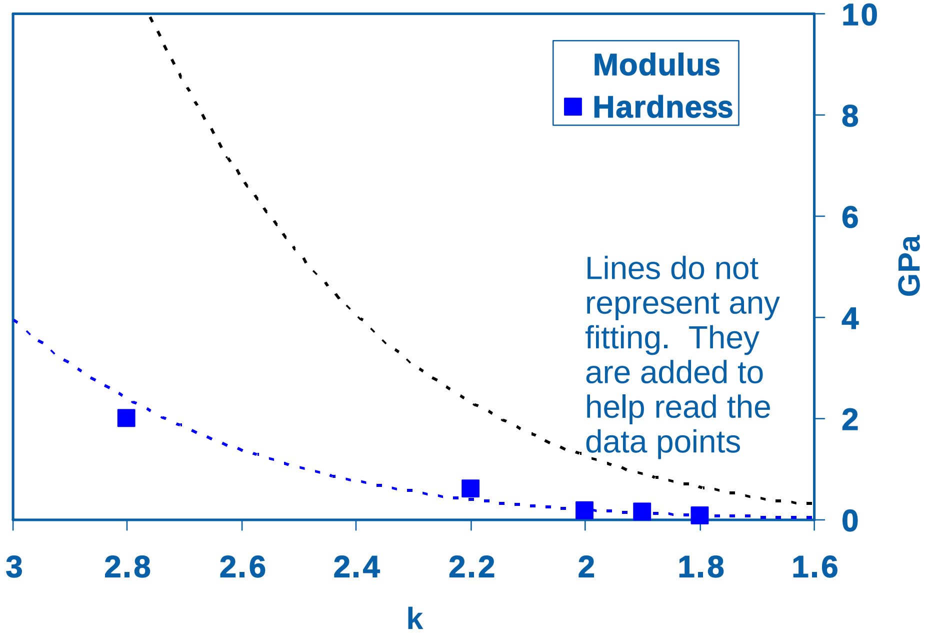


Figure 1. (a) TEM image of free-standing Au nanowires. (b) TEM image of a randomly selected Au wire showing the [111] growth direction and the electron diffraction pattern.

Challenges

- **Control of location and orientation**
- **Control of nanostructure and properties**
- **Reproducibility of nanometer scale contacts**

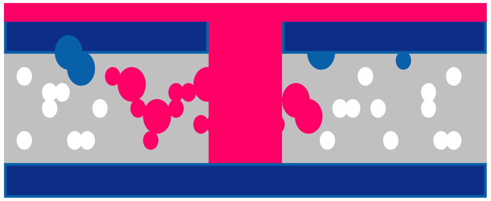
Lower K ILD Required for Future Technologies



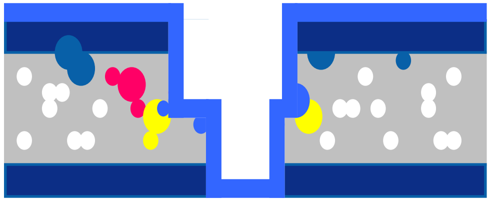
Lines do not represent any fitting. They are added to help read the data points

- Mechanical strength dropping dramatically with lower K
- Reducing K below 2.4 achieved with pores

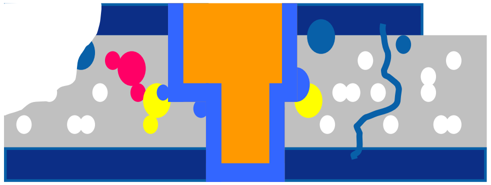
Porous ILD Integration Challenge



Pores are exposed to chemicals in Via Etch



Metal line trench etch exposes pores to even more chemicals



Chemical Mechanical Polish & Packaging

- **Cohesive failure**
- **Cracking**
- **Delamination**

Can novel materials protect pores from chemicals???

Emerging Research Memory

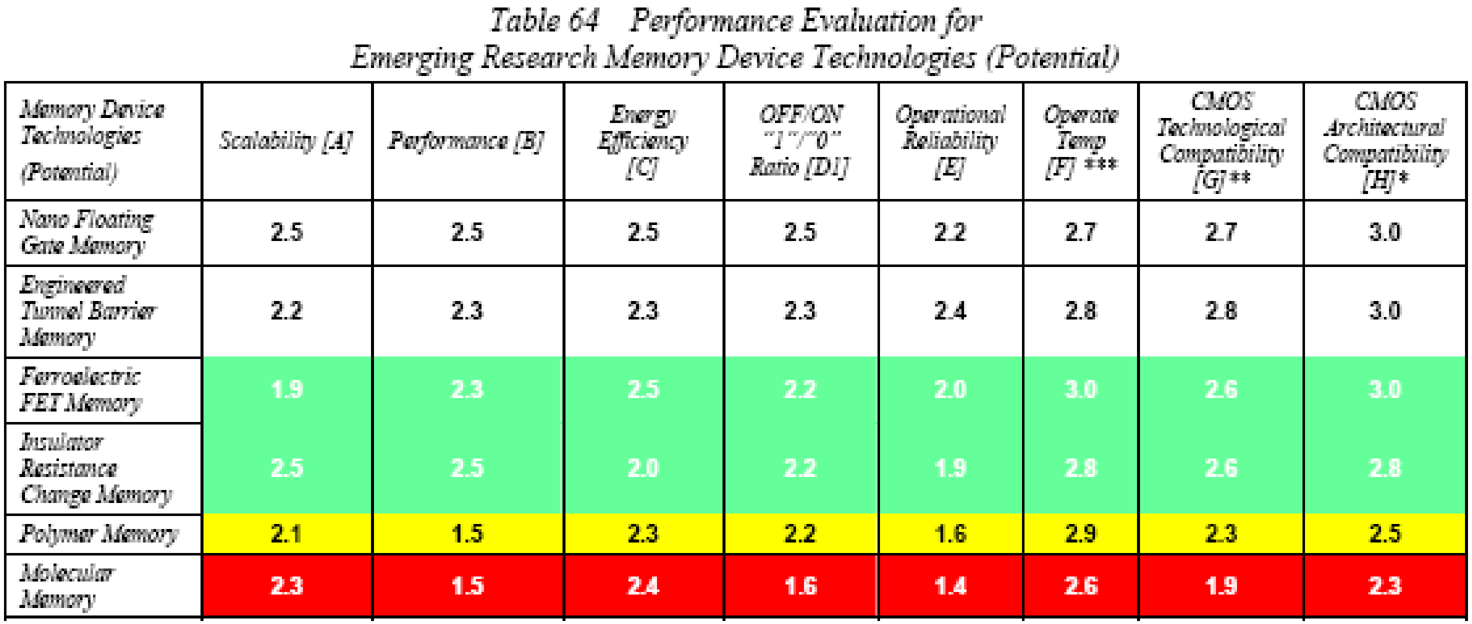


Table 64 Performance Evaluation for Emerging Research Memory Device Technologies (Potential)

Memory Device Technologies (Potential)	Scalability [A]	Performance [B]	Energy Efficiency [C]	OFF/ON "1"/"0" Ratio [D1]	Operational Reliability [E]	Operate Temp [F] ***	CMOS Technological Compatibility [G]**	CMOS Architectural Compatibility [H]*
Nano Floating Gate Memory	2.5	2.5	2.5	2.5	2.2	2.7	2.7	3.0
Engineered Tunnel Barrier Memory	2.2	2.3	2.3	2.3	2.4	2.8	2.8	3.0
Ferroelectric FET Memory	1.9	2.3	2.5	2.2	2.0	3.0	2.6	3.0
Insulator Resistance Change Memory	2.5	2.5	2.0	2.2	1.9	2.8	2.6	2.8
Polymer Memory	2.1	1.5	2.3	2.2	1.6	2.9	2.3	2.5
Molecular Memory	2.3	1.5	2.4	1.6	1.4	2.6	1.9	2.3

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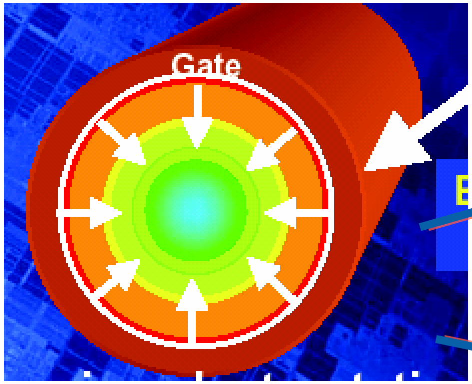
Ferroelectric FET has many material options

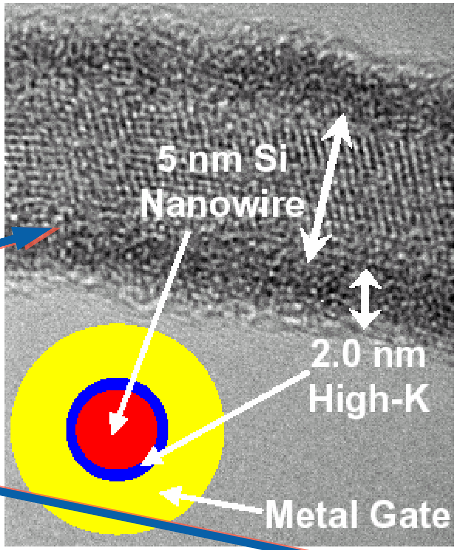
- Combinations of Group II, Transition & Lanthanide oxides

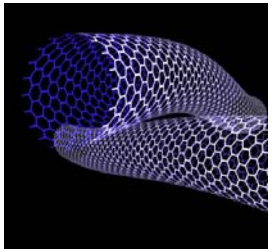
Insulator Resistance Change Memory has many material and mechanism options

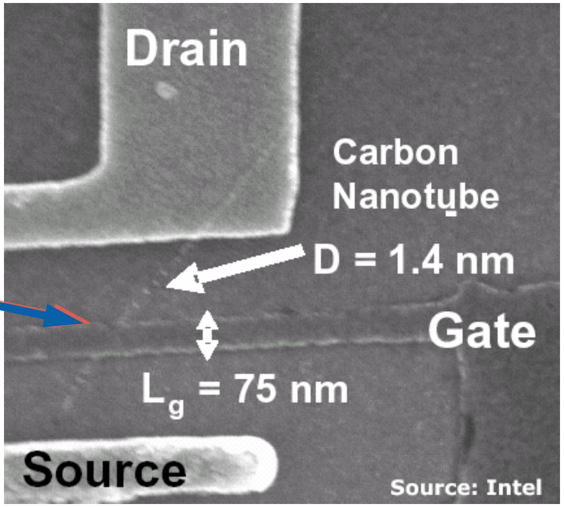
Revolutionary CMOS

Nanomaterial Transistors









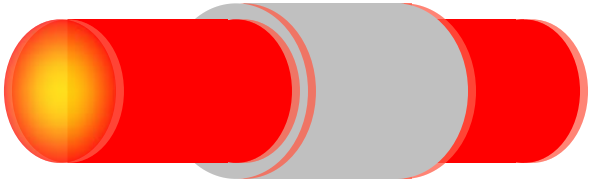
Source: Intel

Options for sub 20nm technologies

Challenges: Placement and property control

Growth Conditions & Catalysts are Critical

1D Characterization & Modeling Challenges



1D Material Challenges

- Control Structure and composition (nm scale)
- Reproducible electronic properties & interactions with interface materials
- nm Scale Placement & Alignment
- Atomic Impurities & Defects
- Wafer & Device Level Property Mapping

Improved Synthesis, Models & Metrology Needed!!!!

Beyond CMOS

Vision: Devices with new functionality integrated with CMOS

What are we looking for?

Required characteristics:

- **Scalability**
- **Performance**
- **Energy efficiency**
- **Gain**
- **Operational reliability**
- **Room temp. operation**

Preferred approach:

- **CMOS process compatibility**
- **CMOS architectural compatibility**

Alternative state variables

Spin–electron, nuclear, photon

Phase

Quantum state

Magnetic flux quanta

Mechanical deformation

Dipole orientation

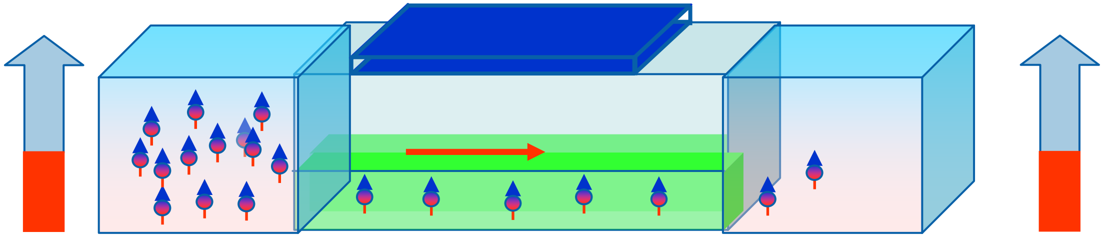
Molecular state

New Nanoscale Devices, Materials & Interfaces

New State Variables: Potential Material Needs

- Materials that support at least 2 stable “states”
- Passivation materials to prevent undesired state changes
- Materials that enable changes of the “state”
- Materials that enable reading the “state” of a device
- Materials to transmit “state” information between “devices”

nm Scale Materials & Characterization



New materials to enable

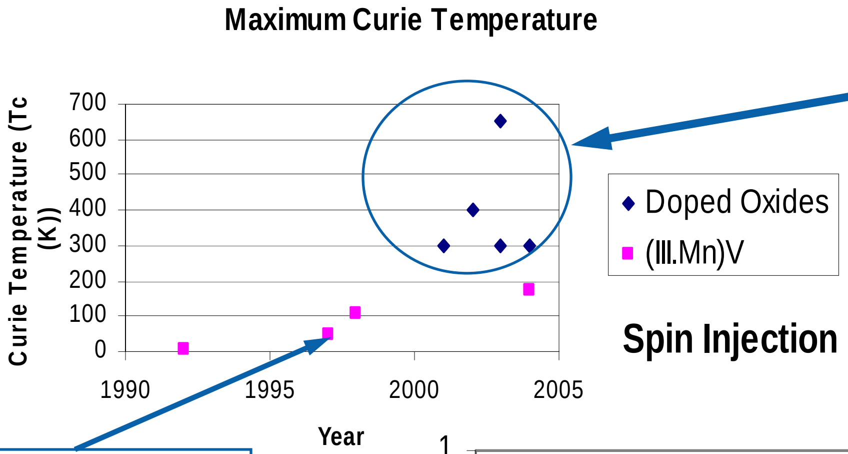
- Room temperature operation
- State amplification (Gain) & transport
- nm Scale devices

New nm scale metrology needs

- State generation, lifetimes, propagation mechanisms, diffusion lengths
  - State interface transport, reflection
  - State coupling & interaction with intrinsic & extrinsic fields

Spin State Material Progress

Room temperature ferromagnetic semiconductors (T curie)

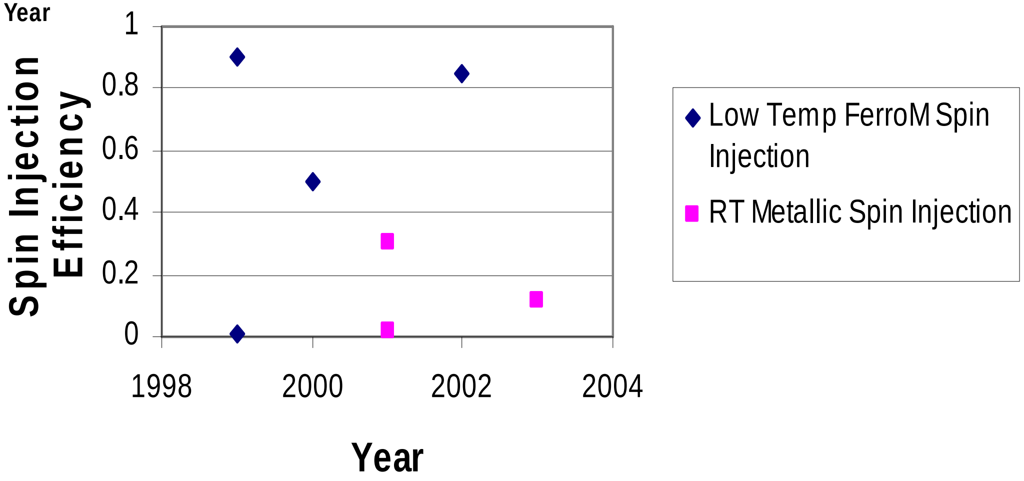


Maximum Curie Temperature

Overlapping Bound Magnetic Polarons, Coey, Nature 2005

Carrier mediated exchange

Spin Injection Efficiency



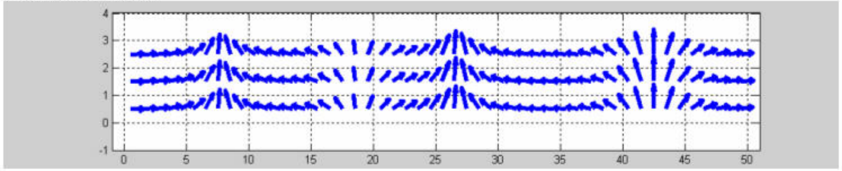
Efficient Spin Injection

Spin GAIN ?????

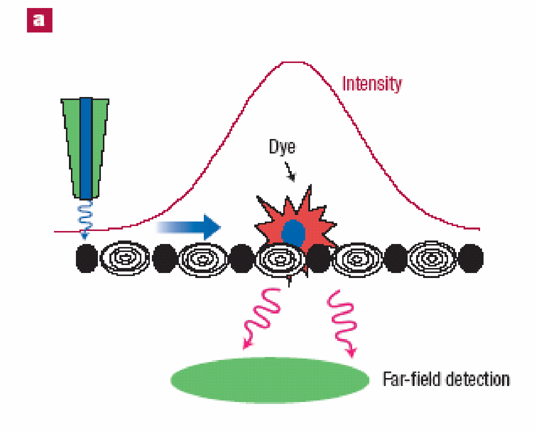
Need Room Temp FM Semiconductor & Spin Gain

Novel short-range energy transfer mechanisms

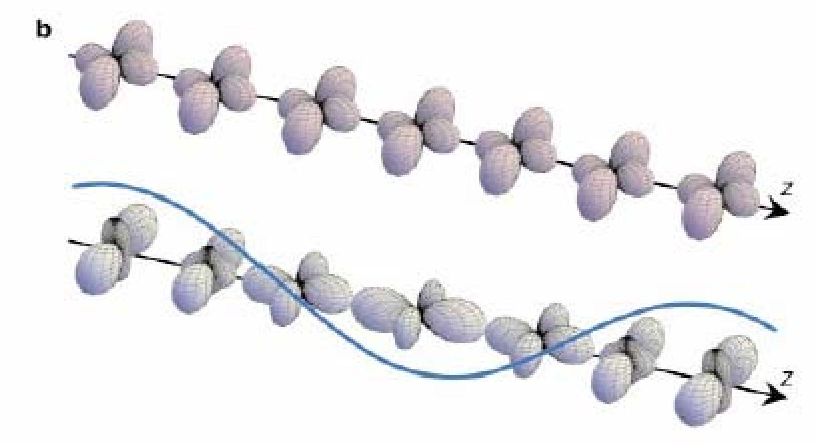
Figure 8. Supporting data. Plan view of the chip. Simulation demonstrating formation of ferromagnetic domains in a wire due to propagation of the spin-orbital wave. This feature provides a natural way for making an inverter.



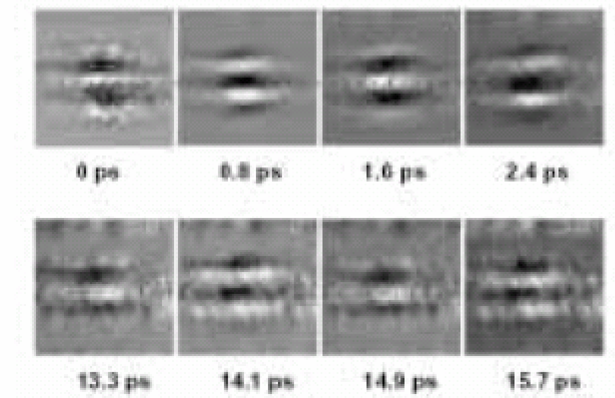
Spin waves, Nikonov, Intel



Plasmons – Atwater, Caltech



Orbitron waves, Tokura, U of Tokyo



Coherent phonons –Stoyananov, MIT

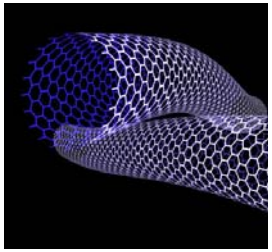
Characterization of coupled phenomena at the nanoscale

Challenges:

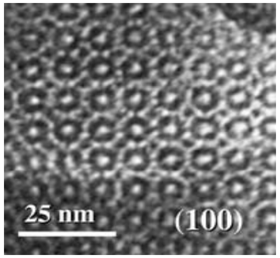
- Resolving single spin, charge and impurities
- Spin wave entanglement and propagation
- Magnetic coupling between and among nano-domains
- Nano-characterization of interface and surface effects
- Novel test structures/methods to deconvolve effects, when possible

Nanomaterial Challenges

Nano-structured Materials

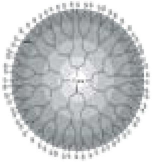


Sub 100nm particles

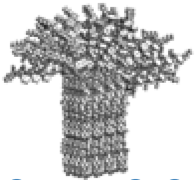


Molecular Assembly (directed & self assembly)

Source: J. Brinker, UNM/Sandia National Labs



Dendrimers



Source: S. Stupp

Macromolecules

Property Control, Contact Resistance and Metrology are Critical

Nano-material Challenges

Significantly improve material performance

Low integration complexity

Controlled assembly into useful forms

Control & reproducibility of properties

Purity

Metrology

Environmental Health & Safety Data

Cost

Nano-materials are often difficult to use!!!

Summary

Summary

Silicon Nanoelectronics is production reality and follows Moore's law

New materials are needed to extend CMOS

Long term: Novel devices will be needed to enhance CMOS

New materials, metrology, and modeling are required

Increased collaboration between Industry, Universities & Gov't is essential!!!